Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **BALANCE**
2. **INPUT –**
3. **INPUT +**
4. **VEE**
5. **BALANCE**
6. **OUTPUT**
7. **VCC**
8. **COMPENSATION**

**.045”**

**5**

**4 3 2**

**1**

**8**

**7**

**6**

**.050”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035 x .0035”**

**Backside Potential: VEE**

**Mask Ref: A**

**APPROVED BY: DK DIE SIZE .045” X .050” DATE: 7/7/22**

**MFG: MOTOROLA THICKNESS .015” P/N: LM748**

**DG 10.1.2**

#### Rev B, 7/1